TABLE I

Incremental Growth at Discontinuities

N	CMA	Type-A	%	Type-B	%	Type-D	%
64→ 65	1→2	8→10	12.5	0→ 5	$\overline{(\infty)}$	2→ 3	-
128→129	2→3	16→19	12.5	8→10	12.5	4→ 5	-
192→193	3→4	24→28	12.5	12→14	8.0	6→ 7	-
256→257	4→5	32→37	12.5	16→19	12.5	8→10	12.5
320→321	5→6	40→46	12.5	20→23	10.0	10→12	10.0
384→385	6→7	48→55	12.5	24→28	12.5	12→14	8.0
448→449	7→8	56→64	12.5	28→32	11.0	14→16	7.0

TABLE II

Number of Type-A Boards Versus Number of PMs if 50% of the Maximum Bandwidth is Maintained (#PMs < 65)

#PMs	#Type-A Boards
2	1
3-8	2
9-18	3
19-32	4
33-40	5
41-48	6
49-56	7
57-64	8

TABLE III

Number of Type-A Boards in the least populated CMA/A Versus Number of PMs if 100% of the Maximum Bandwidth is Maintained (#PMs < 129)

#PMs	#Type-A Boards
2-4	2
5-9	3
10-16	4
17-25	5
26-36	6
37-49	7
50-64	8

TABLE IV

8 x 8 Chip Address Register Bit Definition

BIT	MEANING	DERIVATION
C_{11}	Right/Left	Hardwired on board
$C_{10}C_9$	Stage #	Hardwired on board
$C_8C_7C_6$	Cabinet #	DP supplies it
$C_5C_4C_3$	CMA/A #	DP supplies it
C_5C_4	CMA/B #	DP supplies it
$C_2C_1C_0$	Type-A board #	Hardwired in backplane
$C_3C_2C_1$	Type-B/C board #	Hardwired in backplane
C_0	Type-B/C level	Hardwired on board

TABLE V

Back Channel Merge Logic Results

	Nap	Ack	Nak	Sak	Sense	Count	Sum
Nap	Nap	Ack	Nak	Sak	Sense	Count	Sum
Ack	Ack	Ack	Nak	Sak	Err	Err	Err
Nak	Nak	Nak	Nak	Sak	Err	Err	Err
Sak	Sak	Sak	Sak	Sak	Sak	Sak	Sak
Sense	Sense	Err	Err	Sak	Sense	Err	Err
Count	Count	Err	Err	Sak	Err	Count	Err
Sum	Sum	Err	Err	Sak	Err	Err	Sum